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REMARKS

Claims 5, 21, and 37 have been cancelled. Claims 1, 17, and 32 have been amended.

Claims 1 - 4, 6 - 20, 22 - 32, 33 - 36, and 38 - 48 are pending in this Application.

Reconsideration and further examination is respectfully requested.

Allowable Claims

Claims 6 - 14, 22 - 30, and 38 - 45 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. The Applicant respectfully acknowledges the recognition of the novel subject matter.

Claim Rejections - 35 USC § 103

Claims 1, 4 - 5, 15, 17, 20 - 21, 31 - 32, 36 - 37 and 47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette (US PAT. 6,606,698) in view of Isono et al. (US PAT. 5,892,918 hereinafter "Isono"). Claims 5, 21, and 37 have been cancelled. The rejection with regard to the remaining claims is respectfully traversed.

The Applicant's exemplary claim 1 sets forth:

"A memory interface device for interfacing a number of host applications to a memory device, the memory interface device comprising:

- a host interface for interfacing with the number of host applications in a protocol associated with the corresponding host application;
- a memory interface for interfacing with the memory device wherein one or more of the host applications and the memory device operate in response to different protocols;
- a number of contexts operably coupled to the host interface for receiving memory access requests from the number of host applications and providing

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result/status information to the number of host applications, wherein each host application is associated exclusively with at least one context; and

control logic operably coupled to obtain memory access requests from the number of contexts, translate the memory access requests into memory access requests in accordance with a protocol of the memory device, interact with the memory device over the memory interface for servicing the memory access requests on behalf of the number of host applications, and provide the result/status information to the number of host applications via the number of contexts in accordance with the protocol associated with each of the number of host applications."

An implementation of the Applicants' invention operates to translate requests between multiple different host applications and a memory. Each host application is associated exclusively with at least one of its own contexts that stores the requests and returns result/status information to the host application. Control logic interacts with the contexts to service memory access requests from the applications and return result/status information in accordance with the protocol associated with each host application.

In order to properly maintain a rejection under 35 U.S.C. 103(a), the prior art reference, or references when combined, must teach or suggest all the claim limitations. The Office Action admits, and the Applicants concur, that Fradette fails to teach or suggest the Applicants' claimed "number of contexts ... providing result/status information to the number of host applications".

Note also that Fradette fails to teach the Applicants' contexts as now claimed, wherein each host application is associated exclusively with at least one context, since the clients 30 of Fradette can access all the storage devices and thus all the interface modules 120 and memory regions 126.

(Note also that if one attempts to consider the "host protocols" (unnumbered) of Fradette as the "host applications", then Fradette fails to teach or suggest a memory interface device for interfacing a number of host applications to a memory device, since each device is associated with

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only one protocol.) However, the Office Action asserts that the lists 43 of Isono operate as the claimed contexts. The Applicants respectfully disagree.

Isono describes a system that provides inter-processor communication through the use of lists in a connected device. When one of the logical processing units of Isono, for example 20-10, needs to transfer information to the other logical processing units of Isono, 20-11 and 20-12, the logical processing unit 20-10 puts the information into a list 43. The connecting device 10 then causes the other logical processing units 20-11 and 20-12 to access the list 43 to retrieve the information. Thus, to provide the goal of inter-processor communication, all the logical processing units of Isono have access to all the lists of Isono. Isono therefore fails to teach or suggest the Applicants' claimed memory interface employing "a number of contexts operably coupled to the host interface for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications, wherein each host application is associated exclusively with at least one context".

Since neither Fradette, Isono, nor the combination of the two teach or suggest the claimed memory interface employing "a number of contexts operably coupled to the host interface for receiving memory access requests from the number of host applications and providing result/status information to the number of host applications, wherein each host application is associated exclusively with at least one context, The Applicant respectfully asserts that claim 1 and its dependent claims 4 and 15 are in condition for allowance.

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The Applicant's independent claims 17 and 32 contain limitations analogous to those of claim 1. The Applicant therefore respectfully asserts that claim 17 and its dependent claims 20 and 31, and claim 32 and its dependent claims 33, 36, and 47 are also in condition for allowance.

Claims 2, 16, 18, 34, and 48 were rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette and Isono in view of Wentka et al. (US PAT 5,968,114). This rejection is respectfully traversed.

Claims 2 and 16 are dependent upon claim 1. Claim 18 is dependent upon claim 17. Claims 34 and 48 are dependent upon claim 32. As previously set forth, Fradette and Isono fail to teach or suggest the multiple contexts for receiving memory access requests and providing result/status information to each host application. Wentka adds nothing further to Fradette and Isono that would suggest the claimed multiple contexts. Since Fradette, Isono, and Wentka, taken alone or in combination, fail to teach or suggest the claimed contexts, the Applicant respectfully asserts that claims 2, 16, 18, 34, and 48 are allowable for the reasons set forth with regard to claim 1.

Claims 3, 19, and 35 were rejected under 35 U.S.C. 103(a) as being unpatentable over Fradette and Isono in view of Bauman et al. (US PAT 5,875,472). This rejection is respectfully traversed.

Claim 3 is dependent upon claim 1. Claim 19 is dependent upon claim 17. Claim 35 is dependent upon claim 32. As previously set forth, Fradette and Isono fail to teach or suggest the multiple contexts for receiving memory access requests and providing result/status information to the host applications. Bauman adds nothing further to Fradette and Isono that would suggest the

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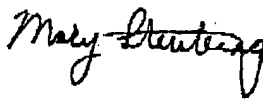
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claimed multiple contexts. Since Fradette, Isono, and Bauman, taken alone or in combination, fail to teach or suggest the claimed contexts, the Applicant respectfully asserts that claims 3, 19, and 35 are allowable for the reasons set forth with regard to claim 1.

Applicants have made a diligent effort to place the rejected claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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Date

Mary Steubing, Reg. No. 37,946
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
125 Nagog Park Drive
Acton, MA 01720
(978) 264-6664

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